Computation Structures

The Digital Abstraction Worksheet

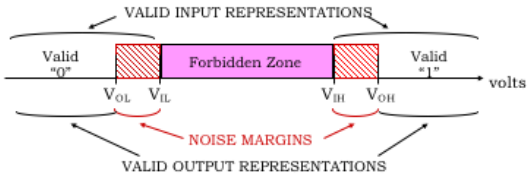
Signaling:

- Analog: each processing step accumulates noise
- Digital: each processing step restores output to a valid digital level

Needed: Noise Margins!

Proposed fix: separate specifications for inputs and outputs

- digital output: "0" ≤ V_{OL}, "1" ≥ V_{OH}
- digital input: "0" ≤ V_{IL}, "1" ≥ V_{IH}
- **$V_{OL} < V_{IL} < V_{IH} < V_{OH}$**



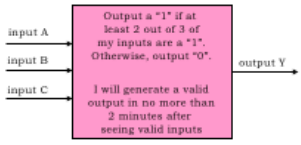
A combinational device accepts marginal inputs and provides unquestionable outputs (to leave room for noise).

A Digital Processing Element

A combinational device is a circuit element that has

Static discipline:

- one or more digital *inputs*
- one or more digital *outputs*
- a *functional specification* that details the value of each output for every possible combination of valid input values
- a *timing specification* consisting (at minimum) of an upper bound t_{PD} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values



A Combinational Digital System

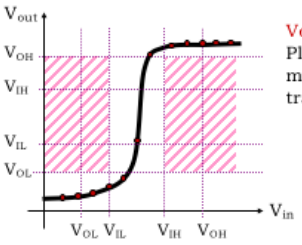
A set of interconnected elements is a combinational device if

- each circuit element is combinational
- every input is connected to exactly one output or to some vast supply of constant 0's and 1's
- the circuit contains no directed cycles

Why is this true?

A Buffer

A simple *combinational device*: 0 → 0 1 → 1



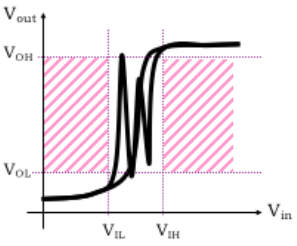
Voltage Transfer Characteristic (VTC): Plot of V_{out} vs. V_{in} where each measurement is taken after any transients have died out.

Note: VTC does not tell you anything about how fast a device is — it measures static behavior not dynamic behavior

Static Discipline requires that the VTC avoid the shaded regions (aka "*forbidden z*[illegible]hich correspond to *valid* inputs but *invalid* outputs.

A Buffer

Voltage Transfer Characteristic



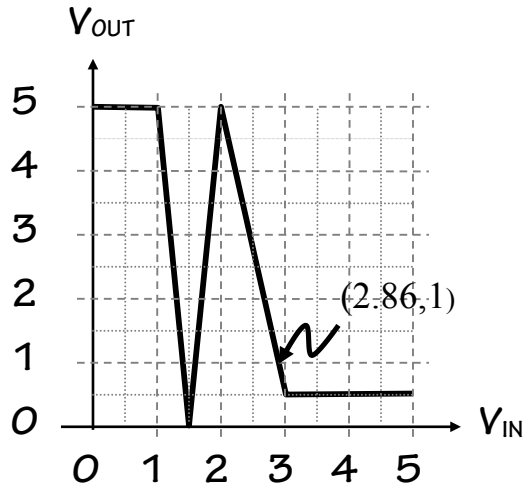
1) Note the VTC can do anything when $V_{IL} < V_{IN} < V_{IH}$.

2) Note that the center white region is taller than it is wide (V_{OH}-V_{OL} > V_{IH}-V_{IL}). Net result: combinational devices must have GAIN > 1 and be NONLINEAR.

Problem 1.

Ms. Anna Logge, founder at a local MIT start-up, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The voltage transfer curve of a proposed inverter for a new logic family is shown to the right (spare copies of this diagram can be found below).



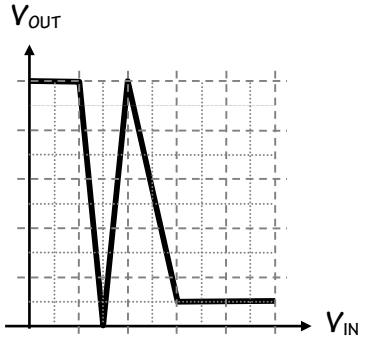
Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. **Recall that Noise Immunity (last row) is defined as the lesser of the two noise margins**.

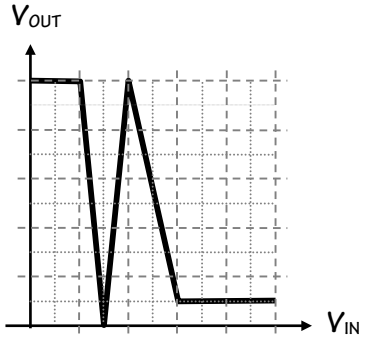
Complete the table by filling in missing entries. Choose each value you enter so as to maximize the noise margins of the corresponding scheme. **If the numbers in a scheme can't be completed such that the device functions as an inverter with positive noise margins, put an X in the entries for that column.**

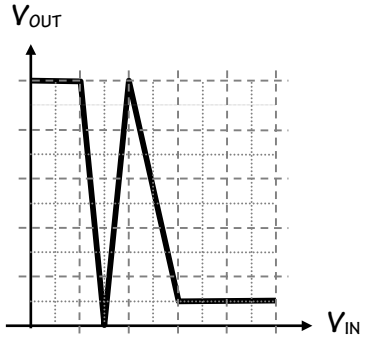
(complete table – 10 entries)

LNI's Possible Logic Mappings:

	Scheme A	**Scheme B**	**Scheme C**
$\mathbf{V_{OL}}$			1
$\mathbf{V_{IL}}$	2	1	0.5
$\mathbf{V_{IH}}$		3	
$\mathbf{V_{OH}}$			
Noise Immunity			

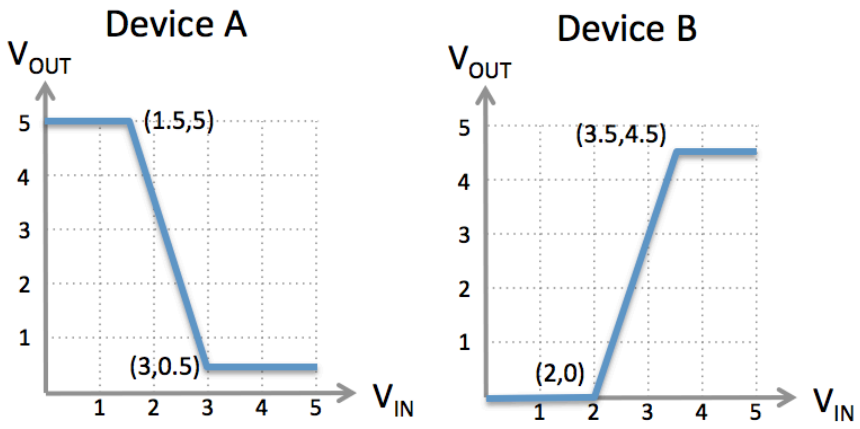






Problem 2.

The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:



Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize the noise immunity (i.e., the smaller of the two noise margins).

V_{OL} = _____ V_{IL} = _____ V_{IH} = _____ V_{OH} = _____

Low Noise Margin = _____ High Noise Margin = _____

Problem 3.

Massachusetts Instruments manufactures the XYZZY family of combinational logic devices, which have the following specifications:

- When signaling a "0" on a device output, XYZZY devices are guaranteed to produce an output voltage of 0.875 ± 0.075 volts.
- When signaling a "1" on a device output, XYZZY devices are guaranteed produce an output voltage of 1.525 ± 0.075 volts.
- XYZZY device inputs compare the incoming voltage against a logic threshold V_{TH}. Input voltages less than or equal to $V_{TH} - 0.05V$ are guaranteed to be interpreted as "0". Input voltages greater than or equal to $V_{TH} + 0.05V$ are guaranteed to be interpreted as "1". V_{TH} is an internal voltage in the range 1.2 ± .1 volts.

(A) Please give the appropriate values for the four digital signaling thresholds:

V_{OL} (volts): _____

V_{IL} (volts): _____

V_{IH} (volts): _____

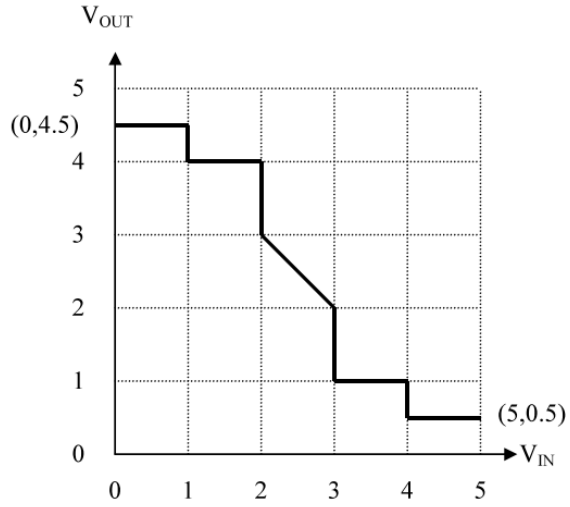
V_{OH} (volts): _____

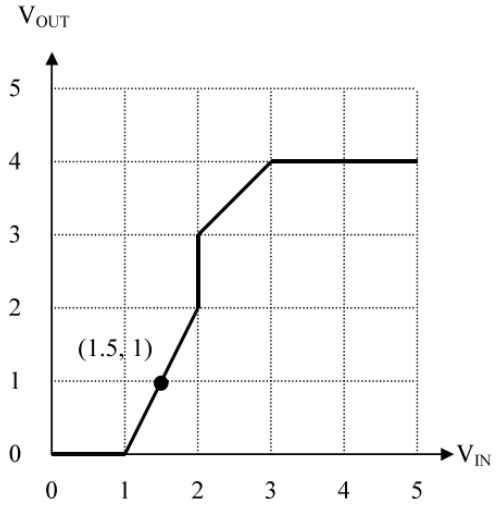
(B) The noise immunity of a signaling specification is the minimum of the two noise margins. What is the noise immunity of your signaling specification?

Noise immunity (volts): _____

Problem 4.

The following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:



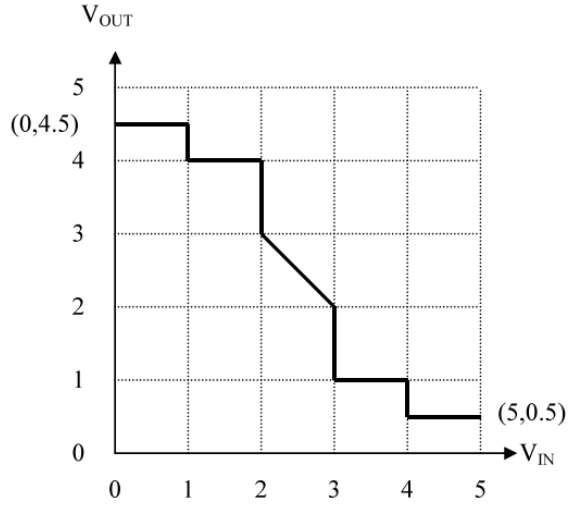


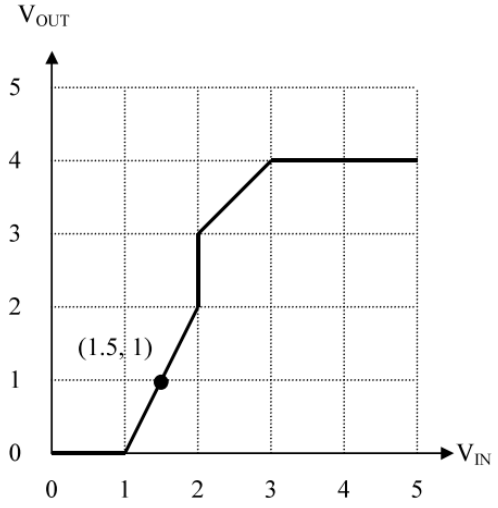
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

V_{OL} = _____ V_{IL} = _____ V_{IH} = _____ V_{OH} = _____

Low Noise Margin = _____ High Noise Margin = _____

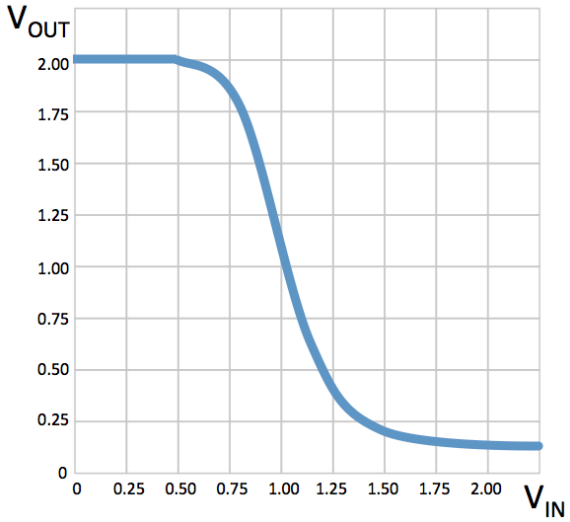
Scratch copy of the VTC diagrams:





Problem 5.

The voltage transfer curve for an NMOS inverter is shown to the right.



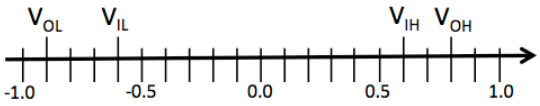
The manufacturer decided to crowd-source the digital signaling specifications for the NMOS inverter and has received some suggestions for V_{OL}, V_{IL}, V_{IH}, and V_{OH}, presented below in tabular form. For each suggested specification determine if the NMOS inverter above would be a legitimate combinational device obeying the static discipline with non-zero positive noise margins. If it is a legitimate combinational device, give the noise immunity of the inverter (the smaller of the low and high noise margins) when operating under that specification. If the inverter wouldn't be a legitimate combinational device, please write NOT LEGIT in the rightmost column.

Fill in rightmost column for each suggested specification.

Suggestion	V_{OL}	V_{IL}	V_{IH}	V_{OH}	*Noise immunity, or NOT LEGIT*
#1	0.00	0.50	1.50	2.00	
#2	0.25	0.75	1.25	1.75	
#3	0.50	0.75	1.25	1.50	
#4	0.75	0.50	1.75	1.50	

Problem 6.

A new family of logic devices uses signaling voltages in the range −1V to +1V. One proposed assignment of our voltage specification is shown below.

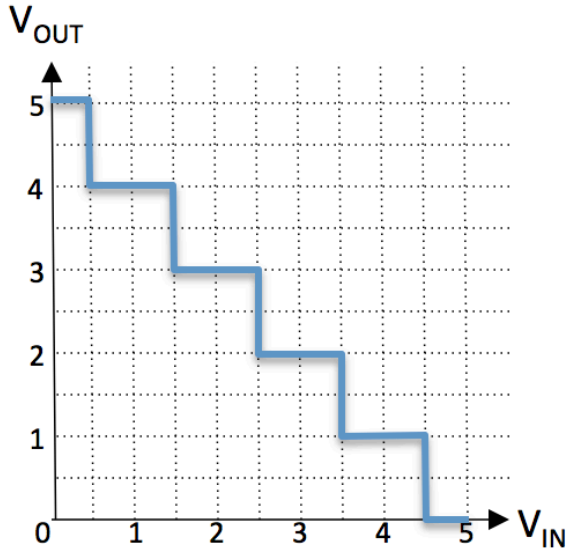


(A) The *noise immunity* of a signaling specification is the smaller of the two noise margins. What is the noise immunity for the signaling scheme proposed above?

(B) The output voltage of an inverter is measured to be 0.9V in the steady state. The inverter is a combinational device obeying the signaling specification shown above. What is the best characterization of the steady-state input voltage V_{IN} of the inverter when the measurement was made?

Problem 7.

Ivan Idea, a resident of Chelyabinsk who's been watching the 6.004 videos on YouTube, was inspired to attach electrodes to opposite ends of a meteor fragment that came through his roof and produce a voltage transfer curve (VTC) of the resulting device, which is shown below.



Amazingly all the "corner points" of the VTC fall on the 0.5V grid.

Ivan is hoping he can sell his device as the world's only extraterrestrial combinational inverter and has provided the table below suggesting possible voltage thresholds to achieve 0.3V noise margins. He's happy to report that for any input voltage, the output voltage becomes stable within 1ns of the application of a new, stable input voltage. For each proposed specification please circle "YES" if the device obeys the static discipline and "NO" if it does not.

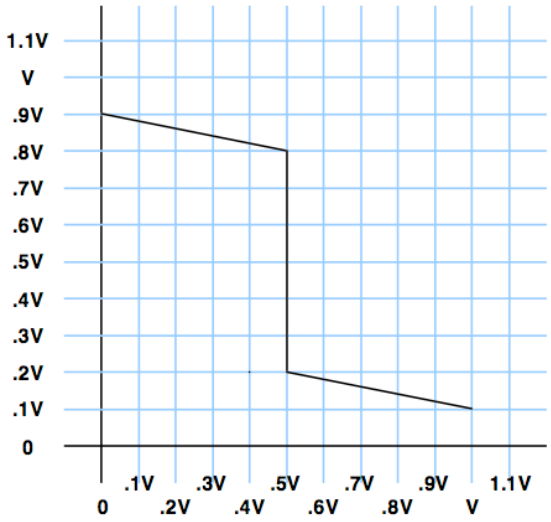
Circle YES or NO for each proposal below

	V_{OL}	V_{IL}	V_{IH}	V_{OH}	Obeys static discipline?
Specification #1	0.1	0.4	4.6	4.9	**YES NO**
Specification #2	0.6	0.9	4.1	4.4	**YES NO**
Specification #3	1.1	1.4	3.6	3.9	**YES NO**

Problem 8.

Consider a device whose voltage transfer characteristic is specified as a function of the supply voltage V as follows

Note that the device has a sharp (infinite gain) threshold at 0.5V.

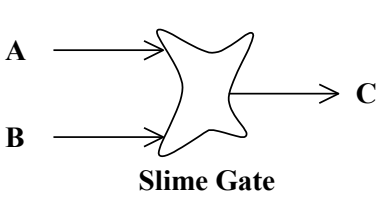


(A) Using this device as an inverter, if V_{OL} is chosen to be 0.2V, what value for V_{IH} will maximize the high noise margin?

(B) What is the maximum noise immunity that can be realized using this device as an inverter, with an appropriately chosen signaling specification?

(C) Suppose manufacturing variations for the above device now allow the threshold voltage to vary between 0.4V and 0.6V, rather than always being 0.5V exactly. If the signaling specifications were adjusted to accommodate this variation, what would be the maximum possible noise immunity?

Problem 9.



Slime Gate

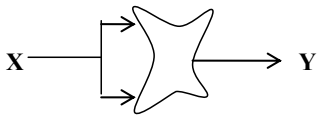
Organic Logic, Inc., is a Cambridge startup that has developed an interesting device built using unidentified organic sludge from the depths of the Charles river; they would like to use it to perform logic functions. Their device, termed a Slime Gate, has two inputs A and B, and one output C (in addition to power and ground connections):

With a 3 volt power supply, they have noted that Slime Gates reliably behave as follows:

- The output C is always in the range 0 volts < C < 3 volts.
- When either (or both) A or B has been less than 1 volt for a nanosecond or more, the voltage at C is greater than 2.5 volts.
- When A and B have both been more than 2 volts for at least a nanosecond, C carries a voltage of less than 0.5 volts.

Aside from the above constraints, the voltage at C is generally unpredictable; it varies widely between individual Slime Gate devices.

As an O.L.I. consultant, you have proposed the following circuit as an inverter in the evolving family of Slime Gate logic:



Inverter

(A) (2 points) Give logic representation parameters yielding 0.5-volt noise margins and for which the above diagram depicts a valid inverter.

V_{OL}: _____; V_{IL}: _____; V_{IH}: _____; V_{OH}: _____

(B) (2 points) Give appropriate specifications for the propagation delay for this inverter.

t_{PD}: _____ ns