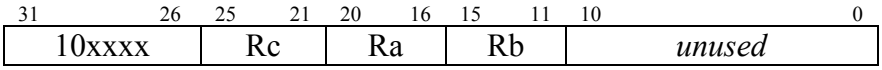
# Summary of β Instruction Formats

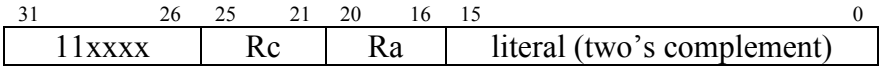
## Operate Class:

| Register | Symbol | Usage |
|---|---|---|
| R31 | R31 | Always zero |
| R30 | XP | Exception pointer |
| R29 | SP | Stack pointer |
| R28 | LP | Linkage pointer |
| R27 | BP | Base of frame pointer |




OP(Ra,Rb,Rc): Reg[Rc] ← Reg[Ra] op Reg[Rb]

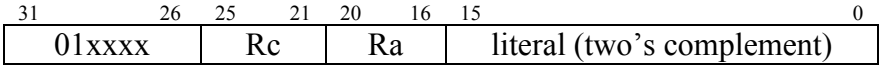
Opcodes: **ADD** (plus), **SUB** (minus), **MUL** (multiply), **DIV** (divided by)
**AND** (bitwise and), **OR** (bitwise or), **XOR** (bitwise exclusive or), **XNOR** (bitwise exclusive nor),
**CMPEQ** (equal), **CMPLT** (less than), **CMPLE** (less than or equal) [result = 1 if true, 0 if false]
**SHL** (left shift), **SHR** (right shift w/o sign extension), **SRA** (right shift w/ sign extension)




OPC(Ra,literal,Rc): Reg[Rc] ← Reg[Ra] op SEXT(literal)

Opcodes: **ADDC** (plus), **SUBC** (minus), **MULC** (multiply), **DIVC** (divided by)
**ANDC** (bitwise and), **ORC** (bitwise or), **XORC** (bitwise exclusive or), **XNORC** (bitwise exclusive nor)
**CMPEQC** (equal), **CMPLTC** (less than), **CMPLEC** (less than or equal) [result = 1 if true, 0 if false]
**SHLC** (left shift), **SHRC** (right shift w/o sign extension), **SRAC** (right shift w/ sign extension)

## Other:




**LD**(Ra,literal,Rc): Reg[Rc] ← Mem[Reg[Ra] + SEXT(literal)]
**ST**(Rc,literal,Ra): Mem[Reg[Ra] + SEXT(literal)] ← Reg[Rc]
**JMP**(Ra,Rc): Reg[Rc] ← PC + 4; PC ← Reg[Ra]
**BEQ**/**BF**(Ra,label,Rc): Reg[Rc] ← PC + 4; if Reg[Ra] = 0 then PC ← PC + 4 + 4*SEXT(literal)
**BNE**/**BT**(Ra,label,Rc): Reg[Rc] ← PC + 4; if Reg[Ra] ≠ 0 then PC ← PC + 4 + 4*SEXT(literal)
**LDR**(label,Rc): Reg[Rc] ← Mem[PC + 4 + 4*SEXT(literal)]

## Opcode Table: (*optional opcodes)

| *2:0*<br>*5:3* | *000* | *001* | *010* | *011* | *100* | *101* | *110* | *111* |
|---|---|---|---|---|---|---|---|---|
| *000* | | | | | | | | |
| *001* | | | | | | | | |
| *010* | | | | | | | | |
| *011* | **LD** | **ST** | | **JMP** | **BEQ** | **BNE** | | **LDR** |
| *100* | **ADD** | **SUB** | **MUL*** | **DIV*** | **CMPEQ** | **CMPLT** | **CMPLE** | |
| *101* | **AND** | **OR** | **XOR** | **XNOR** | **SHL** | **SHR** | **SRA** | |
| *110* | **ADDC** | **SUBC** | **MULC*** | **DIVC*** | **CMPEQC** | **CMPLTC** | **CMPLEC** | |
| *111* | **ANDC** | **ORC** | **XORC** | **XNORC** | **SHLC** | **SHRC** | **SRAC** | |